IEEE Circuits and Systems Society Activity:

"Developing Inter-disciplinary Education in Circuits and Systems Community"

6th March 2014, 10.30-13.00

Dipartimento di Elettronica, Informazione e Bioingegneria

Aula Beta, Edificio 24, Via Golgi 40, Milano

- **10.30-11.15: Michael Peter Kennedy,** University College Cork**:** ***"Digital Delta-Sigma Modulators"***
- **11.15-12.00: Sergio Callegari,** Università di Bologna**:** ***"Convex optimization in the design of the noise shaping features of Delta-Sigma Modulators"***
- **12.00-12.45: Salvatore Levantino,** Politecnico di Milano: ***"The Basics of Digital PLLs".***
- **12.45-13.00: Discussion**

Digital Delta-Sigma Modulators

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Although Digital Delta-Sigma Modulators (DDSMs) are more widely employed commercially than analog DSMs, they are less studied. In particular, issues such as spur generation are not well understood. In the past decade, much progress has been made in this field. This presentation gives a brief introduction to DDSMs for non-specialists, providing insights into the unusual behavior which is often observed in applications. By understanding the root cause of the behavior, novel solutions have been developed to eliminate many of the problems---such as spurs and idle tones---which have historically plagued applications containing DDSMs. Furthermore, by understanding the role of the DDSM in a complete signal processing chain, we show how the concepts of error-masking and bus-splitting can be used in novel architectures to reduce the hardware complexity or to increase the throughput of a channel.

Michael Peter Kennedy is Professor of Microelectronic Engineering at University College Cork (UCC). He received the BE (Electronics) degree from UCD in 1984, the MS and PhD from the University of California at Berkeley in 1987 and 1991, respectively, and the DEng from the National University of Ireland in 2010. He joined UCC as Chair of the Department of Microelectronic Engineering in 2000. He served as Dean of the Faculty of Engineering from 2003 through 2005 and as Vice-President for Research from 2005 to 2011. He has over 340 research publications (including four patents) in the fields of oscillator design, hysteresis, neural networks, nonlinear dynamics, chaos communication, mixed-signal test, and frequency synthesis. He has worked as a consultant for SMEs and multinationals in the microelectronics industry and is founding Director of the Microelectronics Industry Design Association (MIDAS Ireland) and the Microelectronic Circuits Centre of Ireland (MCCI). He was made a Fellow of the Institute of Electrical and Electronic Engineers (IEEE) in 1998 for contributions to the theory of neural networks and nonlinear dynamics and for leadership in nonlinear circuits research and education. He has received many prestigious awards including Best Paper (International Journal of Circuit Theory and Applications), the 88th IEE Kelvin Lecture, IEEE Millenium and Golden Jubilee Medals, the inaugural Royal Irish Academy Parsons Award in Engineering Sciences, and the IEEE Solid-State Circuits Society Chapter of the Year Award 2010. In 2004, he was elected to membership of the Royal Irish Academy and was made a Fellow of the Institution of Engineers of Ireland by Presidential Invitation. From 2005 to 2007, he was President of the European Circuits Society and Vice-President of the IEEE Circuits and Systems (CAS) Society (with responsibility for Europe, Africa and the Middle East). During 2012 and 2013, he was a Distinguished Lecturer of the IEEE CAS Society. He has been Secretary for International Relations of the Royal Irish Academy since 2012. He is currently chair of the PE7 Starter Grants Panel at the European Research Council.

Convex optimization in the design of the noise shaping features of ΔΣ modulators

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ΔΣ modulators can translate an analog, or high-resolution digital input into a low-resolution, high-sample-rate digital signal with minimal loss of fidelity, an activity strategic to many modern applications. This ability owes to their noise shaping features, whose proper design is thus strategic. Historically, there has been a shift from classical architectures, where noise shaping is a mere consequence of a convenient hardware arrangement, to architectures where noise shaping is carefully designed in advance. Yet, current design aids are still limited: in scope, they fail to base their operation on a full vision of the system where the modulator is applied, thus often mistaking requirements; in execution, they often rely on assumptions that only have heuristic or intuitive justifications. In this lecture, current principles of noise shaping design are critically reviewed. It is then illustrated how the noise shaping design can be expressed as an optimization problem. Methods for its recasting in manageable terms via the Kalman–Yakubovich–Popov lemma are proposed, leading to semidefinite programs that can be efficiently solved. Many real world examples are used to illustrate how the novel concepts can lead to higher performance and more versatile architectures, including the design of modulators for signals obtained by frequency-division techniques, the design of audio coders based on psycho-acoustic principles, the design of modulators meant to be embedded in systems whose features can vary. The lecture is interleaved with demos practiced with an open source software toolbox incorporating the techniques under discussion

Sergio Callegari received a Dr. Eng. degree (with honors) in electronic engineering and a Ph.D. degree in electronic engineering and computer science from the University of Bologna, Italy, in 1996 and 2000 respectively, working on the study of nonlinear circuits and chaotic systems. In 1996, he was a visiting student at King's College London, UK. He is currently a researcher and assistant professor at the Department of Electrical, Electronic and Information Engineering (DEI) at the University of Bologna, where he teaches Analog Electronics, Applied Analog Electronics and Sensing to students of Electronic Engineering and Aerospace Engineering. In the same university, he is also a faculty member of the Advanced Research Center on Electronic Systems (ARCES). In 2008, 2009, and 2011 he was for short periods a visiting researcher at the University of Washington in Seattle. His current research interests include nonlinear signal processing, internally nonlinear, externally linear networks, chaotic maps, ΔΣ modulation, testing of analog circuits, and random number generation. Sergio Callegari has authored or co-authored more than 75 papers in international conferences, journals and scientific books, as well as 4 national patents. In 2004 he was co-recipient of the IEEE Circuit and Systems Society Darlington Award, for the best paper appeared in the IEEE Transactions on Circuits and Systems in the previous biennium. He served as an Associate Editor for the IEEE Transactions on Circuits and Systems – Part II during 2006-2007 and as an Associate Editor for the IEEE Transactions on Circuits and Systems – Part I during 2008-2009. He is currently an Associate Editor of the IEICE NOLTA journal. He is Secretary of the Technical Committee on Nonlinear Circuits and Systems and member of the Technical Committee on Education and Outreach, in the IEEE CAS Society. He served in the Organization Committee and as Publication Co-Chair at NOLTA 2006 (Bologna), in the Organization Committee of Eurodoc 2006 (Bologna), as a Special-Session Co-Chair of NOLTA 2010 (Krakow), as a Co-Chair for the nonlinear circuits track at ICECS 2012, as a Chair for the nonlinear circuit track at ISCAS 2013 and as a Co-Chair for the nonlinear circuits and neural network track at ICECS 2013. In 2005-2007, he was a national board member for the Italian Society of Doctoral Candidates and Ph.D. Graduates (ADI).

The Basics of Digital PLLs

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Digital phase-locked loops are establishing themselves as a potential valid alternative to their analog counterpart for the implementation of low-noise frequency synthesizers. One of the main reasons driving this trend is the fact that the area occupation and power consumption of analog loops do not scale down with the technology process. After reviewing the typical analog implementation, this tutorial will introduce the fundamentals of digital phase-locked loops and analyze the mechanisms of generation of limit cycles, which manifest themselves as spurious tones at the output. Then, we will compare two different quantization strategies and develop practical design examples showing how to set loop parameters and optimize phase noise and jitter.

Salvatore Levantino was born in 1973. He received the Laurea degree (cum laude) and the Ph.D. in electrical engineering from the Politecnico di Milano, Italy, in 1998 and 2001, respectively. During the Ph.D., his research interest was focused on fully integrated oscillators and fast-settling frequency synthesizers for wireless applications. From 2000 to 2002 he was a consultant at Bell Labs, Lucent Technologies, Murray Hill (NJ), working on IF-sampling receiver architectures and 5-GHz wireless LAN RF front-ends. Since 2005, he has been Assistant Professor and subsequently Associate Professor of electrical engineering at Politecnico di Milano. He was a lecturer of “Analog Electronics” at Politecnico di Milano (2002-2006) and the instructor of the course of “Integrated Communication Systems” (2004-2010). Since 2010, he has been teaching the graduate course of “RF Circuit Design”. His current research includes wireless transceivers, frequency synthesizers and data converters. Dr. Levantino is co-author of about sixty papers on IEEE journals and conferences and of *Integrated Frequency Synthesizers for Wireless Systems* (Cambridge University Press, 2007). He holds five patents. He served as an associate editor for the *IEEE Transactions on Circuits and Systems II* (2012-2013). Since 2011, he has been serving on the Technical Program Committee for the *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium* and, since 2014, as an associate editor for the *IEEE Transactions on Circuits and Systems I*.