Advanced Topics In Microelectronic Engineering

ATIME 2015/01

Workshop on "Advances in Frequency Synthesis"

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Politecnico di Milano, Italy

Sponsored by the IEEE Circuits and Systems Society Activity: "Inter- and Cross-disciplinary Topics in Circuits and Systems Community"

Monday, 08 June 2015

Auditorium
Analog Devices
Raheen Industrial Estate, Limerick, Ireland

09:00–09:30	Registration
09:30–11:00	Advanced Digital Phase-Locked Loops (Part 1)
11:00–11:30	Break
11:30–13:00	Advanced Digital Phase-Locked Loops (Part 2)
13:00–14:00	Lunch
14:00–15:30	Phase-domain modeling of oscillators: theory and applications

Space is limited so admission is by pre-registration only

If you wish to attend, please email peter.kennedy@ucc.ie
before 18 May 2015 with the subject "ATIME 2015/01"

Advanced Digital Phase-Locked Loops

Salvatore Levantino
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Abstract:

After reviewing the tradeoffs of conventional analog loops, this tutorial will introduce the fundamentals of digital phase-locked loops and analyze the mechanisms of generation of limit cycles, which manifest themselves as spurious tones at the output. Then, we will compare two different quantization strategies and develop practical design examples showing how to set loop parameters and optimize phase noise and jitter. The second part of the tutorial will be devoted to fractional-*N* synthesis, in which quantization and nonlinearity add new sources of spurious tones: We will review the different design techniques which help mitigate such impairments. Finally, examples of state-of-the-art implementations of frequency synthesizers and direct-FM modulators based on digital PLLs will be discussed.

Salvatore Levantino is Associate Professor of Electrical Engineering at Politecnico di Milano, Milan, Italy. His research includes wireless transceivers, frequency synthesizers, and data converters. Author of more than 80 papers on IEEE journals and conferences and the book "*Integrated Frequency Synthesizers for Wireless Systems*" published by CUP in 2007. He is associate Editor of *IEEE TCAS-I* and member of the Steering Committee for the *IEEE RFIC Symposium.*

Phase-domain modeling of oscillators: theory and applications

Paolo Maffezzoni
Politecnico di Milano

Abstract:

Due to circuit complexity, the analysis and design of Analog and Mixed-signal electronics should rely on compact modeling of the functional blocks composing the system and consequent high-level behavioral simulation. In this context, compact macro-modeling of oscillators plays a crucial role. Oscillator macro-models are in fact central to efficiently evaluating the phase-noise performance of PLLs or to investigating synchronization effects in oscillator arrays. In the first part of this talk, we will review the fundamentals of oscillators phase-domain macro-modeling. We will underline how such a technique consists of computing a scalar periodic function that measures the oscillator phase-sensitivity to a given perturbation. Several methods to extract the phase-sensitivity response (PSR) will be presented. In the second part of the talk we will illustrate three applications: a) the analysis of phase-noise mechanism in unconventional oscillator topologies, b) the behavioral phase-noise simulation of digital PLLs and c) the design of multi-phase oscillators.

Paolo Maffezzoni is currently an Associate Professor of electrical engineering at Politecnico di Milano, Italy, where since 2004 he teaches basic Circuit Theory. His research interests include advanced computational methods for the simulation, design and verification of nonlinear circuits and systems, analysis of phase noise and synchronization effects in oscillators, behavioral simulation of analog and mixed-signals systems. On these issues, he has published 62 papers in ISI Journals and 59 papers in peer-referred conferences. Currently, he is serving as an Associate Editor for the *IEEE Transactions on Computer-Aided-Design of Integrated Circuits and Systems* (TCAD) and as a member of the Technical Program Committee of the ACM/IEEE Design Automation Conference (DAC).